IN THE CLAIMS:

Please amend claim 1 as follows.

1. (Currently Amended) A multi-port semiconductor memory comprising;

a memory cell array including a plurality of memory cells,

a first bit line pair performing write-in or read-out of complementary data for said memory cells in said memory cell array,

a second bit line pair performing write-in or read-out of complementary data for said memory cells in said memory cell array,

a plurality of first word lines provided for ~~each of~~ the memory cells for selecting a first memory cell from said memory cell array,

a plurality of second word lines provided to ~~each of~~ said memory cells for selecting a second memory cell from said memory cell array,

and a first pull-up circuit that, when data is written in said first memory cell from said first bit line pair, pulls up low-level of a lower-level line in said first bit line pair.

2. (Previously Presented) The multi-port semiconductor memory according to claim 1 further comprising a first regulator circuit that regulates lower power potential of said first memory cell such that the pull-upped low-level in said first bit line pair is written in said first memory cell as low-level.

3. (Previously Presented) The multi-port semiconductor memory according to claim 1 or 2 further comprising a second pull-up circuit that, when data is written in said second memory cell from said second bit line pair, pulls up ~~a~~ low level of a lower-level line in said second bit line pair.

4. (Previously Presented) The multi-port semiconductor memory according to the claim 3 further comprising a second regulator circuit that regulates lower

power potential of said second memory cell such that the pull-upped low-level in said second bit line pair is written in said second memory cell as low level.

5. (Previously Presented) The multi-port semiconductor memory according to the claim 1, wherein said memory cell comprises:

flip-flop MOS transistors forming a flip-flop storing data, and

gate MOS transistors forming a gate between said flip-flop and said first bit line pair.

6. (Previously Presented) The multi-port semiconductor memory according to the claim 2, wherein said memory cell comprises:

flip-flop MOS transistors forming a flip-flop for storing data, and

gate MOS transistors forming a gate between said flip-flop and said first bit line pair

wherein said first regulator circuit comprises MOS transistor for switching between said gate MOS transistors and a ground line.

7. (Previously Presented) The multi-port semiconductor memory according to the claim 1, wherein said first pull-up circuit comprises:

a first MOS transistor having a source connected to one bit line in said first bit line pair, a drain connected to a power line and a gate inputted a write-in enable signal, and

a second MOS transistor having a source connected to another bit line in said first bit line pair, a drain connected to a power line and a gate inputted a write-in enable signal.

8. (Previously Presented) The multi-port semiconductor memory according to the claim 3, wherein said second pull-up circuit comprises:

a first MOS transistor having a source connected to one bit line in said second bit line pair, a drain connected to a power line and a gate inputted a write-in enable signal, and

a second MOS transistor having a source connected to another bit line in said second bit line pair, a drain connected to a power line and a gate inputted a write-in enable signal.

9. (Previously Presented) The multi-port semiconductor memory according to the claim 4, wherein said memory cell comprises:

flip-flop MOS transistors forming a flip-flop for storing data, and

gate MOS transistor forming a gate between said flip-flop and said first bit line pair

wherein said second regulator circuit comprises MOS transistor for switching between said gate MOS transistors and a ground line.